Kodak

DEVICE
PERFORMANCE
SPECIFICATION

KODAK KAI-11000M
KODAK KAI-11000CM
Image Sensor

4008 (H) x 2672 (V)
Interline Transfer
Progressive Scan CCD

June 2, 2003
Revision 3.0

www.kodak.com/go/imagers 585-722-4385 Email: imagers@kodak.com

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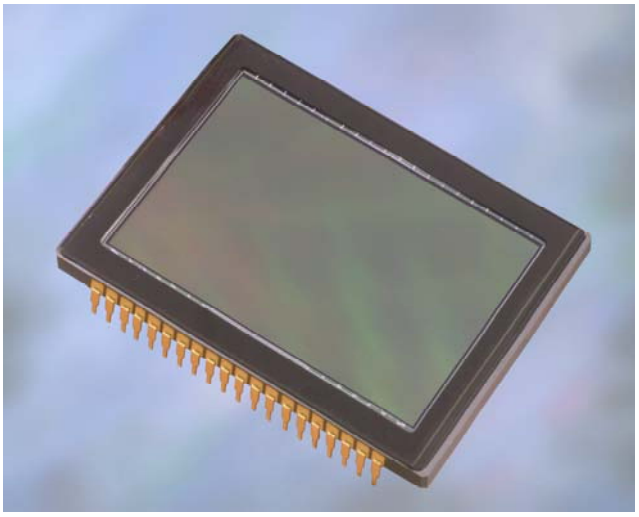
KODAK KAI-11000 Image Sensor 4008 (H) x 2672 (V) Interline Transfer Progressive Scan CCD



Description

The Kodak KAI-11000 Image Sensor is a high-performance 11-million pixel sensor designed for professional digital still camera applications. The 9.0 µm square pixels with microlenses provide high sensitivity and the large full well capacity results in high dynamic range. The two high-speed outputs and binning capabilities allow for 1-3 frames per second (fps) video rate for the progressively scanned images. The vertical overflow drain structure provides antiblooming protection and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.

Parameter	Value
Architecture	Interline CCD; Progressive Scan
Total Number of Pixels	4072 (H) x 2720 (V) = approx. 11.1M
Number of Effective Pixels	4032 (H) x 2688 (V) = approx. 10.8M
Number of Active Pixels	4008 (H) x 2672 (V) = approx. 10.7M
Number of Outputs	1 or 2
Pixel Size	9.0µm (H) x 9.0µm (V)
Imager Size	43.3mm (diagonal)
Chip Size	37.25mm (H) x 25.70mm (V)
Aspect Ratio	3:2
Saturation Signal	60,000 electrons
Quantum Efficiency (KAI-11000M)	50%
Quantum Efficiency (KAI-11000CM) RGB	34%, 37%, 42%
Output Sensitivity	13 µV/e
Total Noise	30 electrons
Dark Current	< 50 mV/s
Dark Current Doubling Temperature	7 ºC
Dynamic Range	66 dB
Charge Transfer Efficiency	> 0.99999
Blooming Suppression	> 1000X
Smear	< -80 dB
Image Lag	< 10 electrons
Maximum Data Rate	28 MHz
Package	40-pin, CerDIP, 0.070” pin spacing
Cover Glass	AR Coated

All parameters above are specified at T = 40*C

REVISION NO.: 3
EFFECTIVE DATE: June 3, 2003

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DEVICE DESCRIPTION

Architecture

Overall

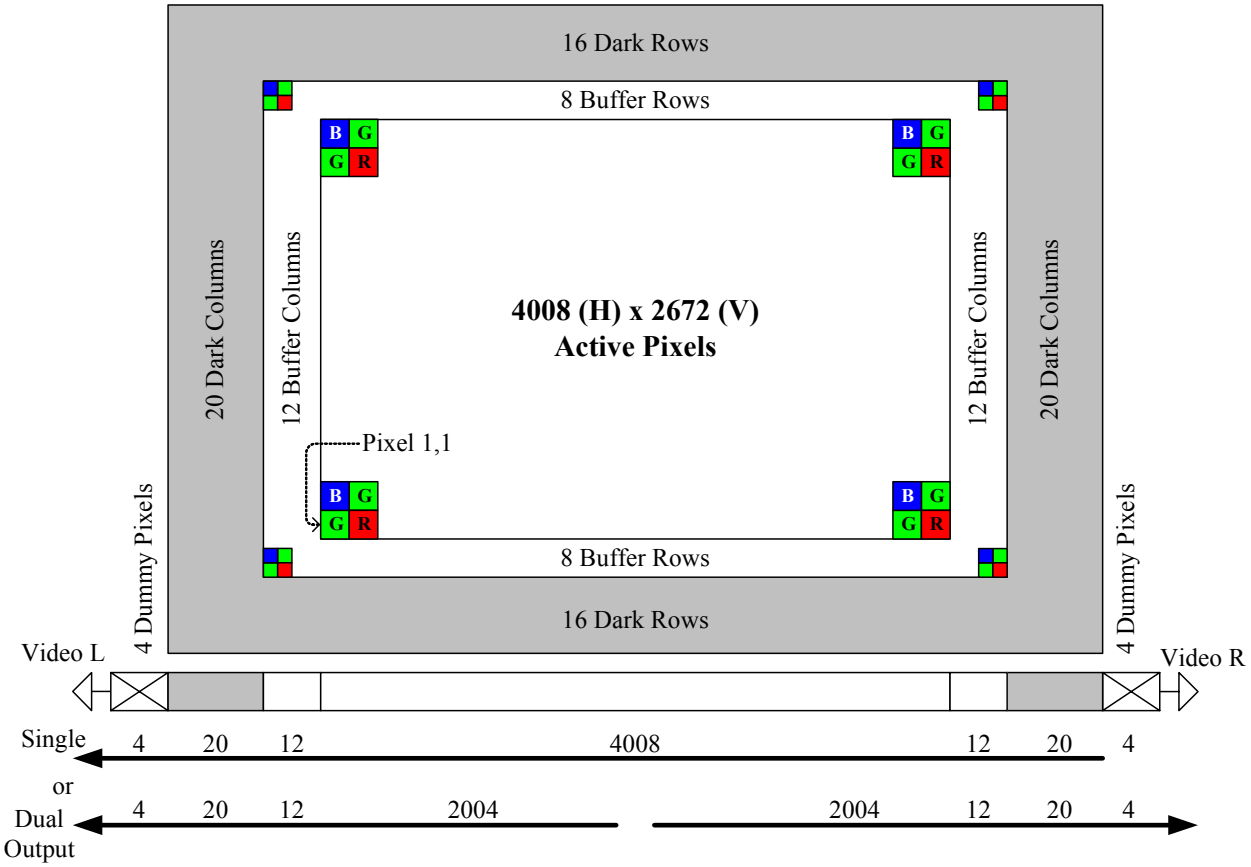


Figure 1 - Sensor Architecture

There are 16 light shielded rows followed 2688 photoactive rows and finally 16 more light shielded rows. The first 8 and the last 8 photoactive rows are buffer rows giving a total of 2672 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first 4 empty pixels of each line do not receive charge from the vertical shift register. The next 20 pixels receive charge from the left light shielded edge followed by 4032 photosensitive pixels and finally 20 more light shielded pixels from the right edge of the sensor. The first and last 12 photosensitive pixels are buffer pixels giving a total of 4008 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. Each row consists of 4 empty pixels followed by 20 light shielded pixels followed by 2016 photosensitive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

Pixel

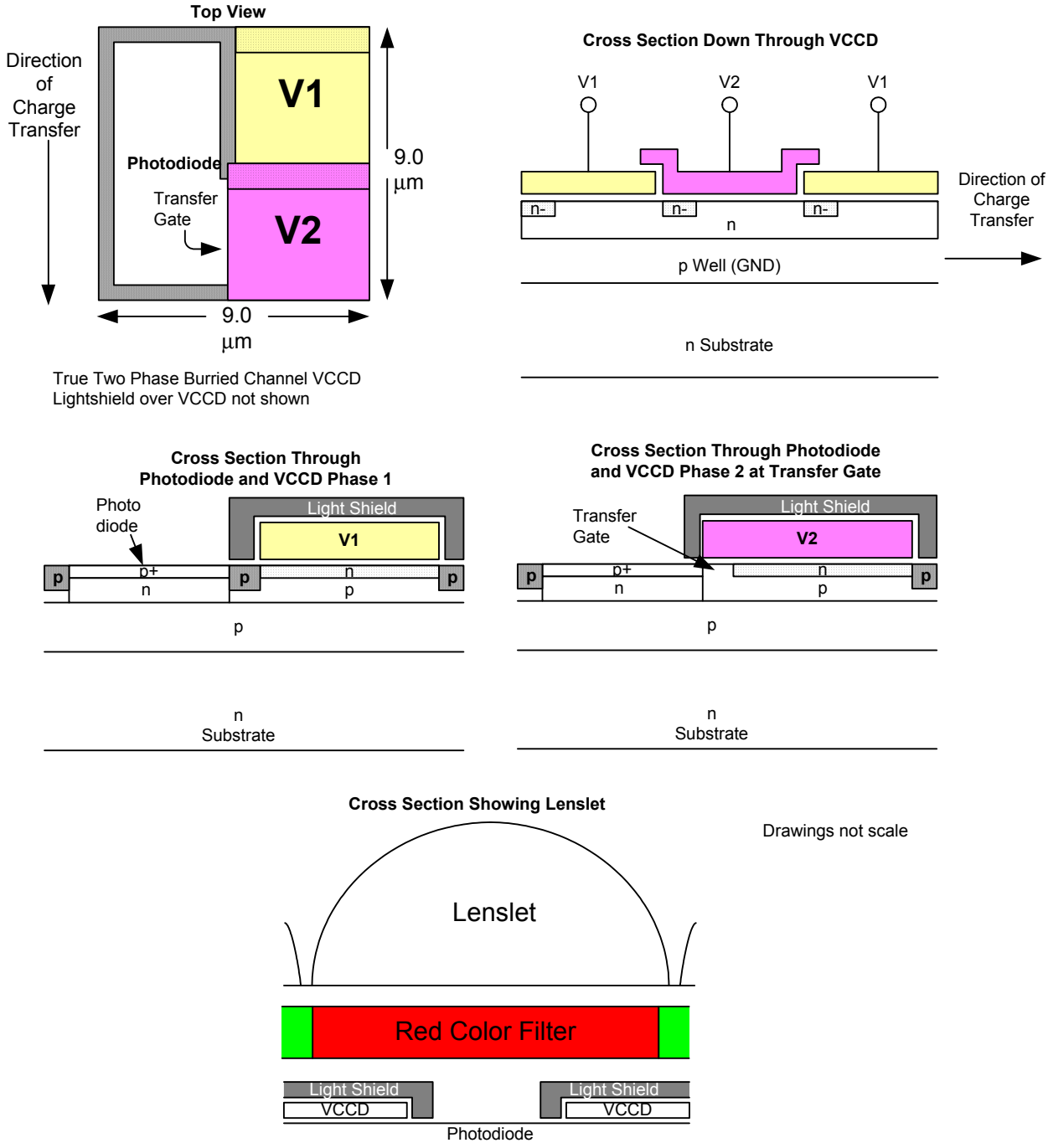


Figure 2 - Pixel Architecture

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependant upon light level and exposure time and non-linearly dependant on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Vertical to Horizontal Transfer

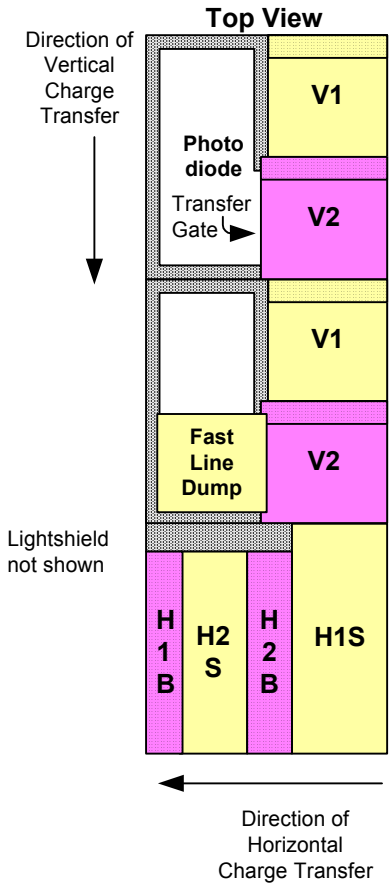


Figure 3 - Vertical to Horizontal Transfer Architecture

When the V1 and V2 timing inputs are pulsed, charge in every pixel of the VCCD is shifted one row towards the HCCD. The last row next to the HCCD is shifted into the HCCD. When the VCCD is shifted, the timing signals to the HCCD must be stopped. H1 must be stopped in the high state and H2 must be stopped in the low state. The HCCD clocking may begin THD µs after the falling edge of the V1 and V2 pulse.

Charge is transferred from the last vertical CCD phase into the H1S horizontal CCD phase. Refer to Figure 20 for an example of timing that accomplishes the vertical to horizontal transfer of charge.

If the fast line dump is held at the high level (FDH) during a vertical to horizontal transfer, then the entire line is removed and not transferred into the horizontal register.

Horizontal Register to Floating Diffusion

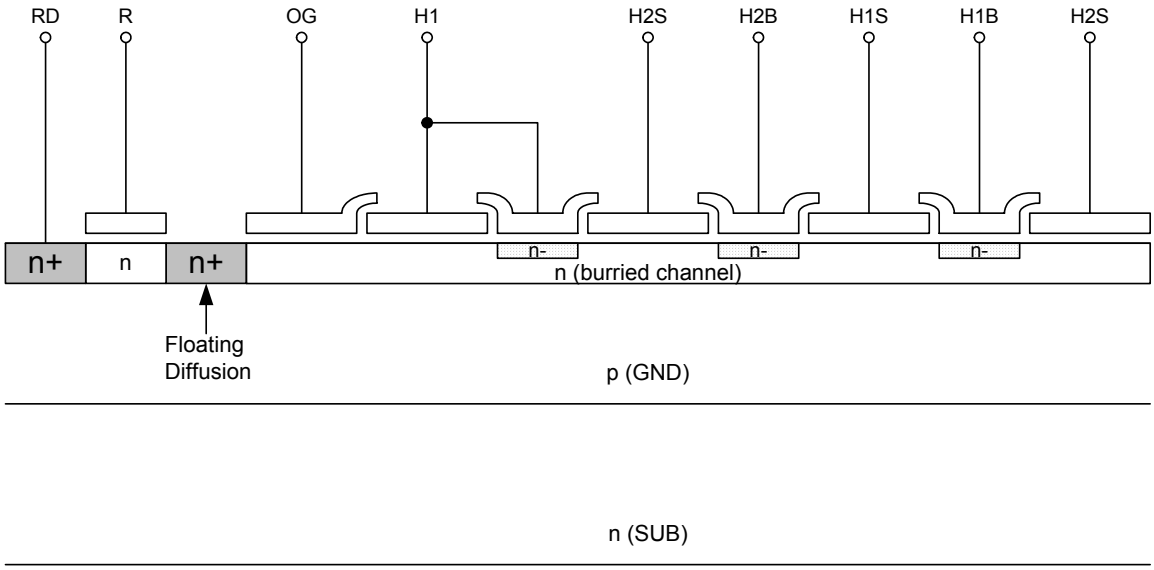


Figure 4 - Horizontal Register to Floating Diffusion Architecture

The HCCD has a total of 4080 pixels. The 4072 vertical shift registers (columns) are shifted into the center 4072 pixels of the HCCD. There are 4 pixels at both ends of the HCCD, which receive no charge from a vertical shift register. The first 4 clock cycles of the HCCD will be empty pixels (containing no electrons). The next 20 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. The next 4032 clock cycles will contain photo-electrons (image data). Finally, the last 20 clock cycles will contain only electrons generated by dark current in the VCCD and photodiodes. Of the 20 dark columns, the first and last dark columns should not be used for determining the zero signal level. Some light does leak into the first and last dark columns. Only use the center 18 columns of the 20 column dark reference.

When the HCCD is shifting valid image data, the timing inputs to the electronic shutter (SUB), VCCD (V1, V2), and fast line dump (FD) should be not be pulsed. This prevents unwanted noise from being introduced. The HCCD is a type of charge coupled device known as a pseudo-two phase CCD. This type of CCD has the ability to shift charge in two directions. This allows the entire image to be shifted out to the video L output, or to the video R output (left/right image reversal). The HCCD is split into two equal halves of 2040 pixels each. When operating the sensor in single output mode the two halves of the HCCD are shifted in the same direction. When operating the sensor in dual output mode the two halves of the HCCD are shifted in opposite directions. The direction of charge transfer in each half is controlled by the H1BL, H2BL, H1BR, and H2BR timing inputs.

Horizontal Register Split

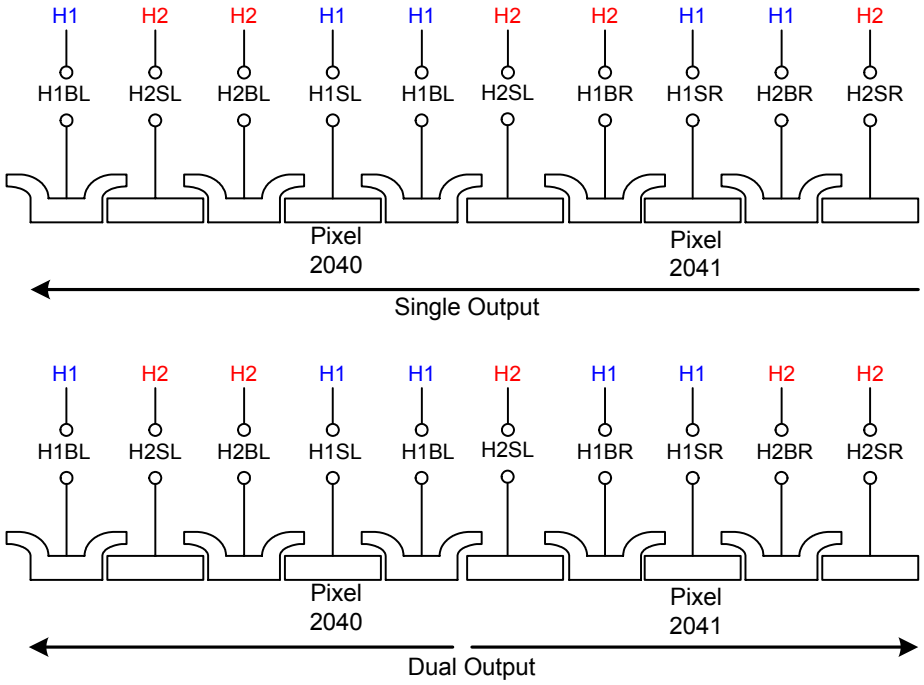


Figure 5 - Horizontal Register

Single Output Operation

When operating the sensor in single output mode all pixels of the image sensor will be shifted out the Video L output (pin 2). To conserve power and lower heat generation the output amplifier for Video R may be turned off by connecting VDDR (pin 18) and VOUTR (pin 19) to GND (zero volts).

The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H2BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H1BR. In other words, the clock driver generating the H1 timing should be connected to pins 8, 9, 13, and 11. The clock driver generating the H2 timing should be connected to pins 7, 10, 14, and 12. The horizontal CCD should be clocked for 4 empty pixels plus 20 light shielded pixels plus 4032 photoactive pixels plus 20 light shielded pixels for a total of 4076 pixels. H1BINL and H1BINR use the H1 timing, but should be generated from a separate clock driver for optimal performance.

Dual Output Operation

In dual output mode the connections to the H1BR and H2BR pins are swapped from the single output mode to change the direction of charge transfer of the right side horizontal shift register. In dual output mode both VDDL and VDDR (pins 3, 18) should be connected to 15 V. The H1 timing from the timing diagrams should be applied to H1SL, H1BL, H1SR, H1BR, and the H2 timing should be applied to H2SL, H2BL, H2SR, and H2BR. The clock driver generating the H1 timing should be connected to pins 8, 9, 13, and 12. The clock driver generating the H2 timing should be connected to pins 7, 10, 14, and 11. The horizontal CCD should be clocked for 4 empty pixels plus 20 light shielded pixels plus 2016 photoactive pixels for a total of 2040 pixels. If the camera is to have the option of dual or single output mode, the clock driver signals sent to H1BR and H2BR may be swapped by using a relay. Another alternative is to have two extra clock drivers for H1BR and H2BR and invert the signals in the timing logic generator. If two extra clock drivers are used, care must be taken to ensure the rising and falling edges of the H1BR and H2BR clocks occur at the same time (within 3ns) as the other HCCD clocks.

Output

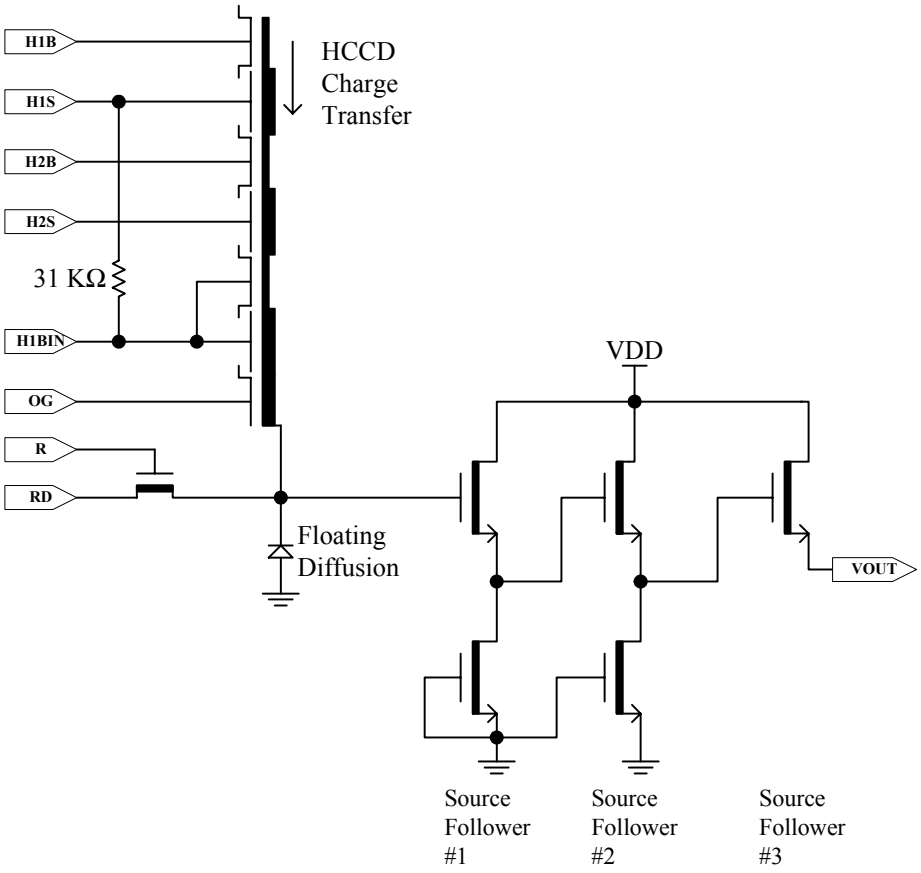
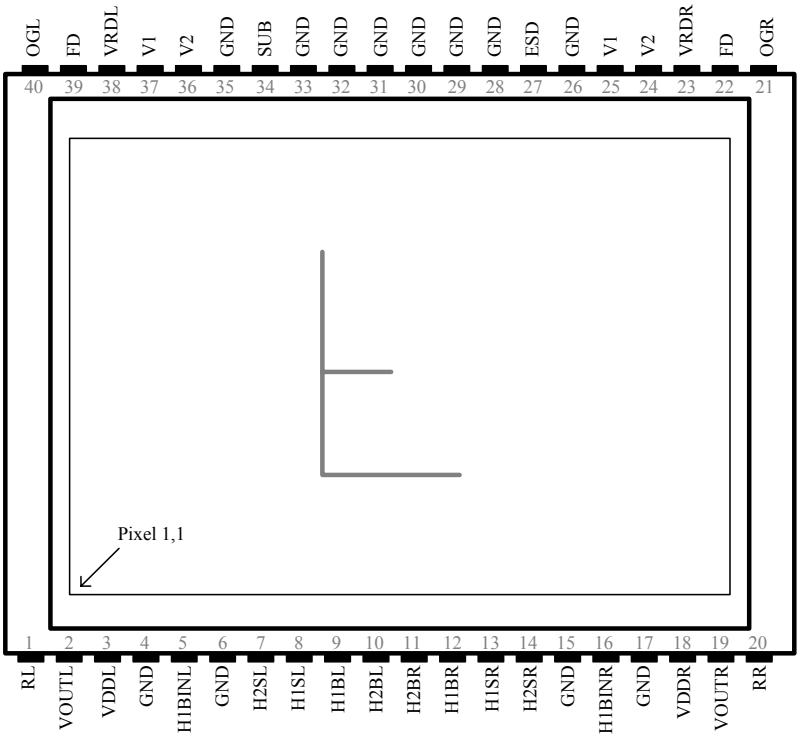


Figure 6 - Output Architecture

Charge packets contained in the horizontal register are dumped pixel by pixel onto the floating diffusion (fd) output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential charge is determined by the expression $\Delta Vfd=\Delta Q/Cfd$. A three-stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of microvolts per electron ($\mu V/e^-$). After the signal has been sampled off chip, the reset clock (R) removes the charge from the floating diffusion and resets its potential to the reset drain voltage (RD).

Physical Description

Pin Description and Device Orientation



Pin	Name	Description	Pin	Name	Description
1	RL	Reset Gate, Left	**40**	OGL	Output Gate, Left
2	VOUTL	Video Output, Left	**39**	FD	Fast Line Dump Gate
3	VDDL	Vdd, Left	**38**	RDL	Reset Drain, Left
4	GND	Ground	**37**	V1	Vertical Clock, Phase 1
5	H1BINL	H1 Last Phase, Left	**36**	V2	Vertical Clock, Phase 2
6	GND	Ground	**35**	GND	Ground
7	H2SL	H2 Storage, Left	**34**	SUB	Substrate
8	H1SL	H1 Storage, Left	**33**	GND	Ground
9	H1BL	H1 Barrier, Left	**32**	GND	Ground
10	H2BL	H2 Barrier, Left	**31**	GND	Ground
11	H2BR	H2 Barrier, Right	**30**	GND	Ground
12	H1BR	H1 Barrier, Right	**29**	GND	Ground
13	H1SR	H1 Storage, Right	**28**	GND	Ground
14	H2SR	H2 Storage, Right	**27**	ESD	ESD Protection
15	GND	Ground	**26**	GND	Ground
16	H1BINR	H1 Last Phase, Right	**25**	V1	Vertical Clock, Phase 1
17	GND	Ground	**24**	V2	Vertical Clock, Phase 2
18	VDDR	Vdd, Right	**23**	RDR	Reset Drain, Right
19	VOUTR	Video Output, Right	**22**	FD	Fast Line Dump Gate
20	RR	Reset Gate, Right	**21**	OGR	Output Gate, Right

The pins are on a 0.07” spacing

PERFORMANCE

Power - Estimated

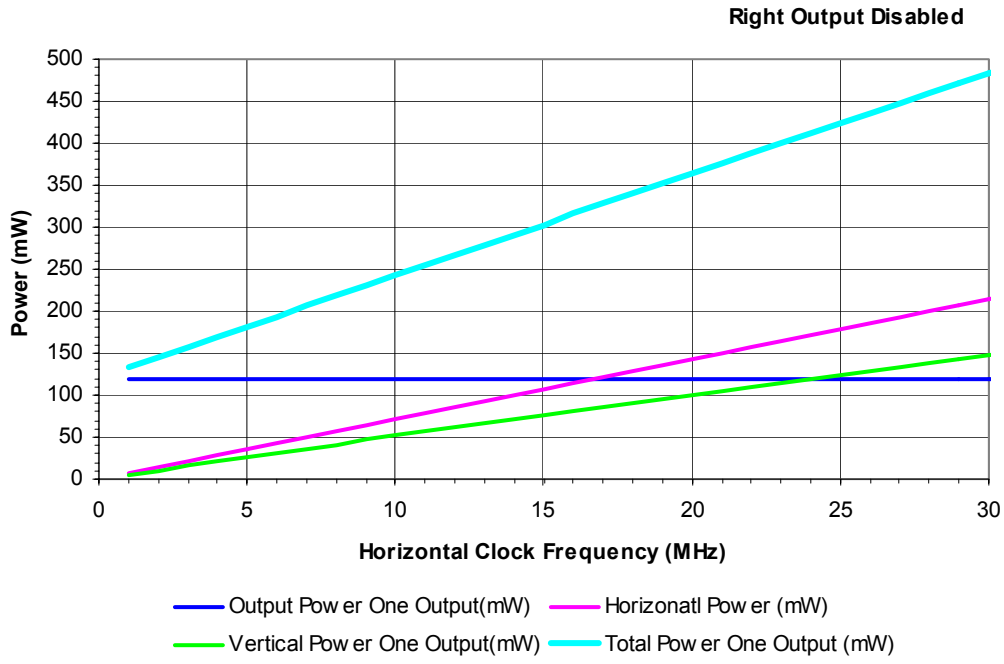


Figure 7 - Power

Frame Rates – Continuous Mode

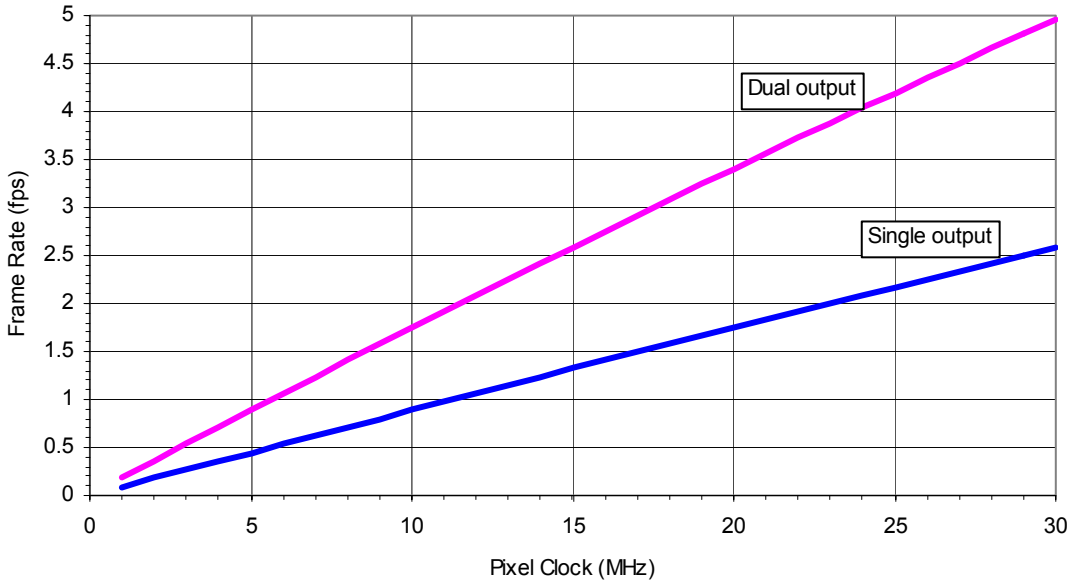


Figure 8 - Frame Rates

Imaging Performance

Image Performance Operational Conditions

Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions:

Description	Condition	Notes
Frame time	1732 msec	1
Horizontal clock frequency	10 MHz	
Light source (LED)	Continuous red, green and blue illumination centered at 450, 530 and 650 nm	2, 3
Operation	Nominal operating voltages and timing	

Notes:
1. Electronic shutter is not used. Integration time equals frame time.
2. LEDs used: Blue: Nichia NLPB500, Green: Nichia NSPG500S and Red: HP HLMP-8115.
3. For monochrome sensor, only green LED used.

Imaging Performance Specifications

KAI-11000M and KAI-11000CM

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes	Test
Maximum Photoresponse Nonlinearity	NL	n/a	2		%	Design		2, 3	
Maximum Gain Difference Between Outputs	ΔG	n/a	10		%	Design		2, 3	
Max. Signal Error due to Nonlinearity Dif.	ΔNL	n/a	1		%	Design		2, 3	
Horizontal CCD Charge Capacity	HNe		139		ke^-	Design			
Vertical CCD Charge Capacity	VNe	90	91		ke^-	Die			
Photodiode Charge Capacity	PNe	58	60		ke^-	Die			
Horizontal CCD Charge Transfer Efficiency	HCTE	0.99999		n/a		Design			
Vertical CCD Charge Transfer Efficiency	VCTE	0.99999		n/a		Design			

Description (cont)	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes	Test
Photodiode Dark Current	Ipd	n/a		800	e/p/s	Die			
Photodiode Dark Current	Ipd	n/a		0.15	nA/cm^2	Die			
Vertical CCD Dark Current	Ivd	n/a		3800	e/p/s	Die			
Vertical CCD Dark Current	Ivd	n/a		0.5	nA/cm^2	Die			
Image Lag	Lag	n/a	<10	50	e^-	Design			
Antiblooming Factor	Xab	100	300	n/a		Design			
Vertical Smear	Smr	n/a	-85	-75	dB	Design			
Total Noise	n_{e-T}		30		e^-rms	Design		4	
Dynamic Range	DR		66		dB	Design		5	
Output Amplifier DC Offset	V_{odc}	4	9	14	V	Die			
Output Amplifier Bandwidth	F_{-3db}		106		MHz	Die		6	
Output Amplifier Impedance	R_{OUT}	100	150	200	Ohms	Die			
Output Amplifier Sensitivity	$\Delta V/\Delta N$		13		$\mu V/e^-$	Design			

KAI-11000M

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes	Test
Peak Quantum Efficiency	QE_{max}	45	50	n/a	%	Design			
Peak Quantum Efficiency Wavelength	λQE	n/a	500	n/a	nm				

KAI-11000CM

Description	Symbol	Min.	Nom.	Max.	Units	Sampling Plan	Temperature(s) Tested At (°C)	Notes	Test
Peak Quantum Efficiency Red Green Blue	QE_{max}		34 37 42	n/a n/a n/a	%	Design			
Peak Quantum Efficiency Wavelength Red Green Blue	λQE		630 550 470	n/a n/a n/a	nm	Design			

n/a: not applicable

Notes:
1. Per color.
2. Value is over the range of 10% to 90% of photodiode saturation.
3. Value is for the sensor operated without binning
4. Includes system electronics noise, dark pattern noise and dark current shot noise at 30 MHz.
5. Uses 20LOG(PNe/ n_{e-T})
6. Last stage only, Cload=10pF. Then $f_{-3db} = (1 / (2\pi * R_{out} * C_{load}))$

Defect Definitions

Description	Definition	Class 1 Maximum Color or Monochrome	Class 2 Maximum Color Only	Temperature(s) tested at (°C)	Notes	Test
Major dark field defective pixel	Defect >= 239 mV	100	200	27, 40	1	1
Major bright field defective pixel	Defect >= 15 %				1	2
Minor dark field defective pixel	Defect >= 123 mV	1000	2000	27, 40	1	1
Cluster defect	A group of 2 to 10 contiguous major defective pixels, but no more than 3 adjacent defects horizontally	20	20	27, 40	1	
Column defect	A group of more than 10 contiguous major defective pixels along a single column	0	10	27, 40	1	

Notes:
1. There will be at least two non-defective pixels separating any two major defective pixels.

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All pixels are referenced to pixel 1,1 in the defect map.

Quantum Efficiency

Color with Microlens Quantum Efficiency

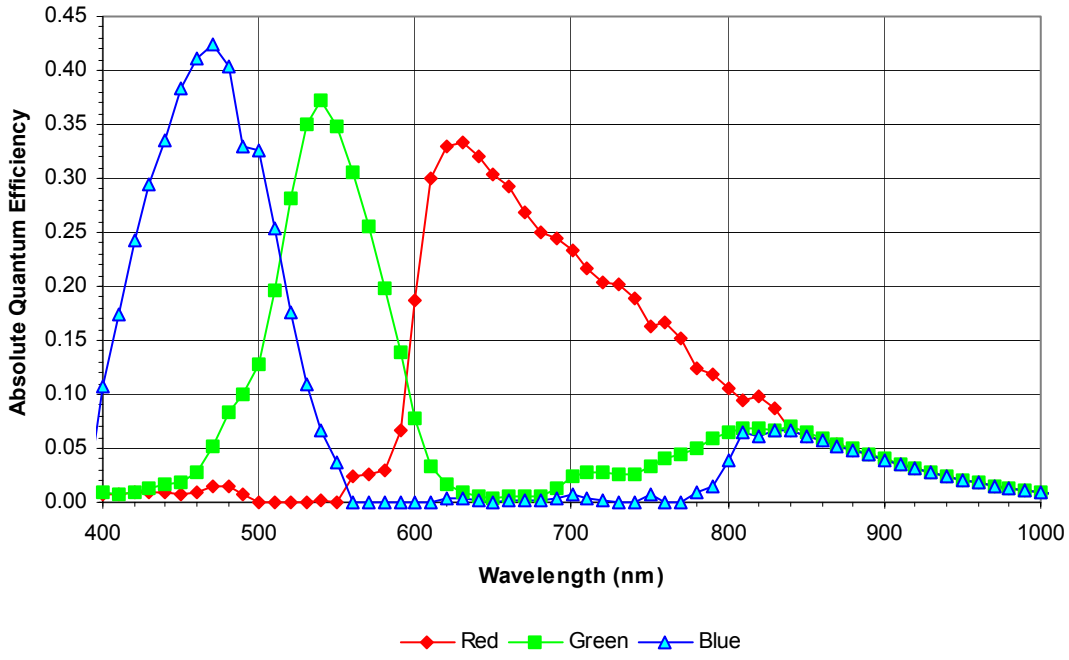


Figure 9 - Color with Microlens Quantum Efficiency Using AR Glass

Monochrome with Microlens Quantum Efficiency

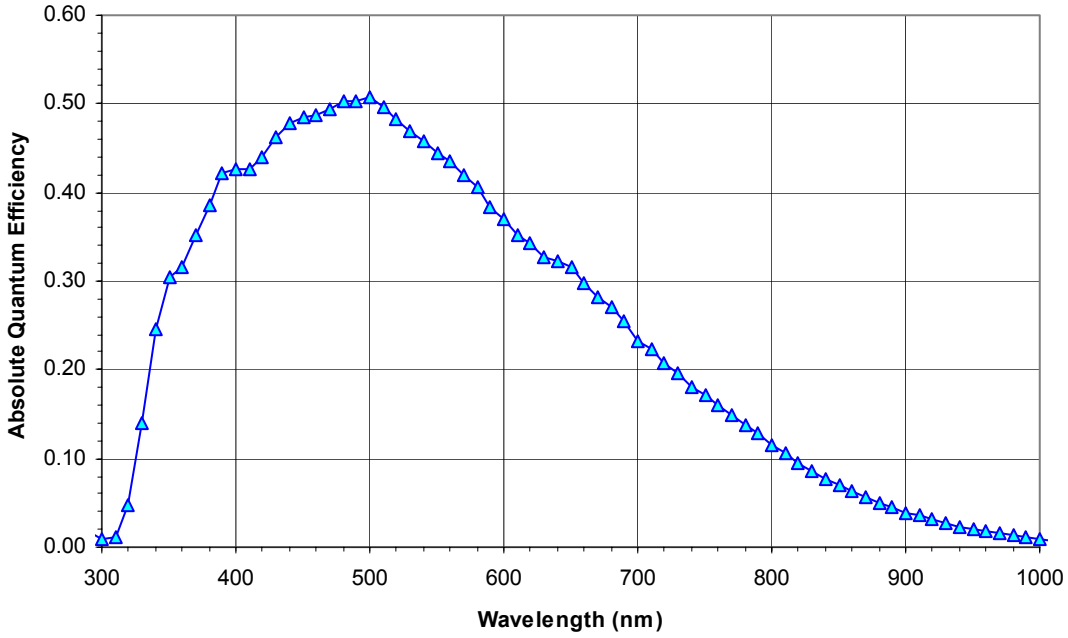


Figure 10 - Monochrome with Microlens Quantum Efficiency

Angular Quantum Efficiency

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD. For the curve marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

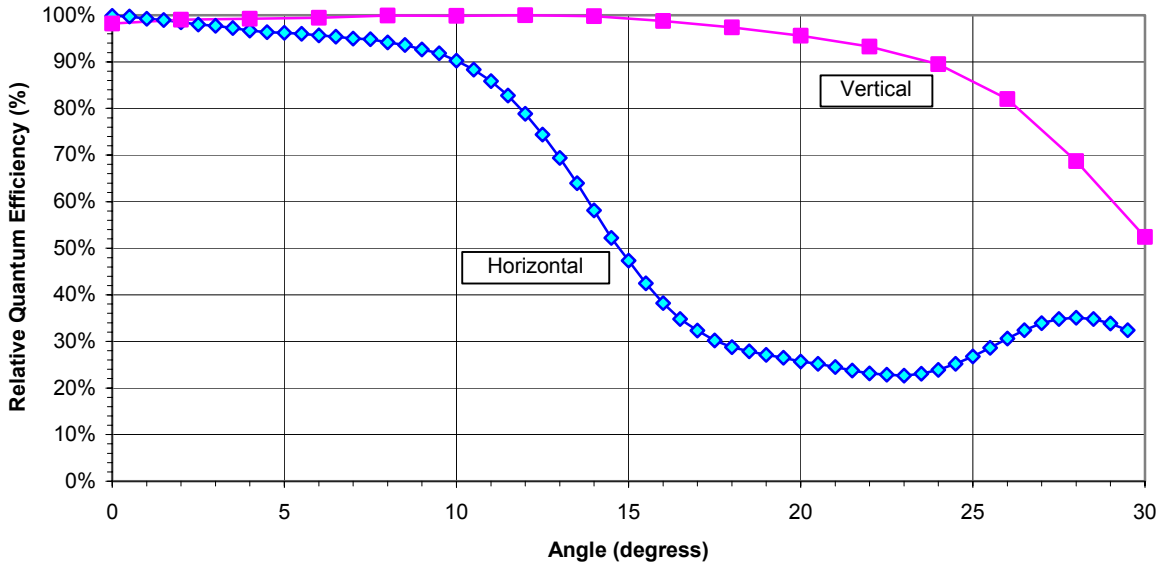


Figure 11 - Angular Quantum Efficiency

TEST DEFINITIONS

Test Regions of Interest

Active Area ROI: Pixel 1, 1 to Pixel 4008,2672
Center 100 by 100 ROI: Pixel 1954,1336 to Pixel 2053,1435

Only the active pixels are used for performance and defect tests.

OverClocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 12 for a pictorial representation of the regions.

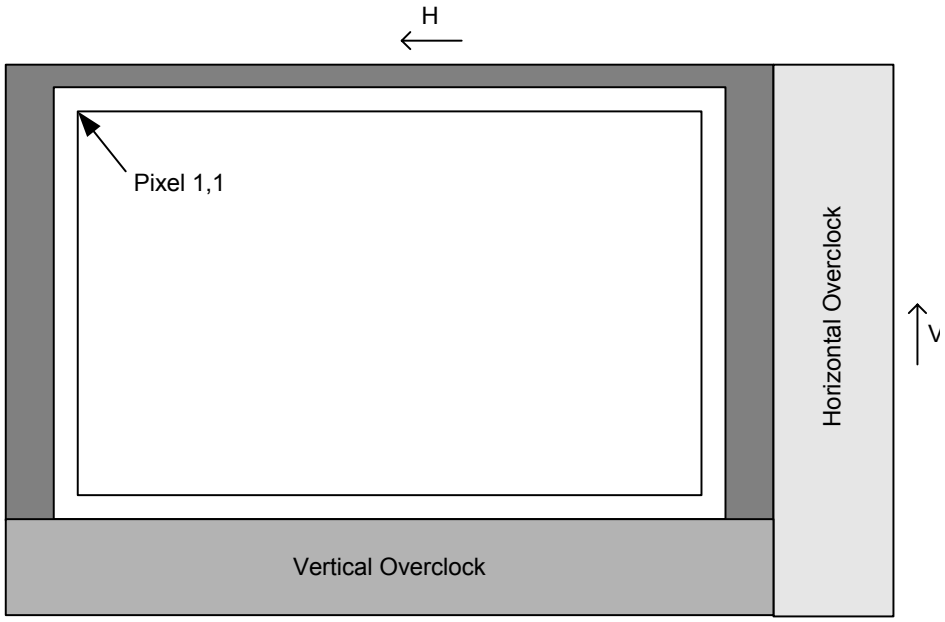


Figure 12 - Overclock Regions of Interest

Tests

1. **Dark field defect test**
   This test is performed under dark field conditions. The sensor is partitioned into 384 sub regions of interest, each of which is 167 by 167 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the "Defect Definitions" section.

2. **Bright field defect test**
   This test is performed with the imager illuminated to a level such that the output is at approximately 40,000 electrons. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 60,000 electrons. The average signal level of all active pixels is found. The bright and dark thresholds are set as:
   Dark defect threshold = Active Area Signal * threshold
   Bright defect threshold = Active Area Signal * threshold

   The sensor is then partitioned into 384 sub regions of interest, each of which is 167 by 167 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.
   Example for major bright field defective pixels:
   - Average value of all active pixels is found to be 520 mV (40,000 electrons).
   - Dark defect threshold: 520mV * 15% = 78 mV
   - Bright defect threshold: 520mV * 15% = 78 mV
   - Region of interest #1 selected. This region of interest is pixels 1,1 to pixels 167,167.
     - Median of this region of interest is found to be 520 mV.
     - Any pixel in this region of interest that is >= (520+78 mV) 598 mV in intensity will be marked defective.
     - Any pixel in this region of interest that is <= (520-78 mV) 442 mV in intensity will be marked defective.
   - All remaining 384 sub regions of interest are analyzed for defective pixels in the same manner.

OPERATION

Maximum Ratings

Description	Symbol	Minimum	Maximum	Units	Notes
Operating Temperature	T_{OP}	-50	70	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	Iout	0.0	-40	mA	3
Off-chip Load	C_L		10	pF	

Notes:
1. Noise performance will degrade at higher temperatures.
2. T=25ºC. Excessive humidity will degrade MTTF.
3. Total for both outputs. Current is -20 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
4. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Caution: This device contains limited protection against Electrostatic Discharge (ESD).
Devices should be handled in accordance with strict ESD procedures for Class 0 devices (JESD22 Human Body Model) or Class A (Machine Model). Refer to Application Note MTD/PS-0224, “Electrostatic Discharge Control”

Caution: Improper cleaning of the cover glass may damage these devices.
Refer to Application Note MTD/PS-0237, “Cover Glass Cleaning for Image Sensors”

Caution: Each sensor is shipped with a protective tape on the cover glass. Care should be used when removing the tape to prevent ESD damage. The tape should be removed when the sensor is in the shipping container or when the sensor is in a camera.

DC Bias Operating Conditions

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Output Gate	OG	-3.0	-2.5	-2.0	V	1 µA	
Reset Drain	RD	10.5	11.5	11.5	V	1 µA	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	2 mA	
Ground	GND	0.0	0.0	0.0	V		
Substrate	SUB	8.0	TBD	17.0	V		1
ESD Protection	ESD	-9.0	-8.0	-7.0	V		2
Output Bias Current	Iout		-5	-10	mA		3

Notes:
1. The operating of the substrate voltage, Vab, will be marked on the shipping container for each device. The value of Vab is set such that the photodiode charge capacity is 60,000 electrons.
2. VESD must be at least 1 V more negative than H1L and H2L during sensor operation *AND* during camera power turn on.
3. An output load sink must be applied to Vout to activate output amplifier.

AC Operating Conditions

Clock Levels

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Vertical CCD Clock High	V2H	7.5	8.0	8.5	V	
Vertical CCD Clocks Midlevel	V1M, V2M	-0.2	0.0	0.2	V	
Vertical CCD Clocks Low	V1L, V2L	-9.5	-9.0	-8.5	V	
Horizontal CCD Clocks Amplitude	H1H, H2H	5.8	6.0	6.2	V	
Horizontal CCD Clocks Low	H1L, H2L	-4.2	-4.0	-3.8	V	
Reset Clock High	RH	1.3	1.5	1.7	V	
Reset Clock Low	RL	-3.7	-3.5	-3.3	V	
Electronic Shutter Voltage	Vshutter	39	40	48	V	
Fast Dump High	FDH	4.5	5.0	5.5	V	
Fast Dump Low	FDL	-9.5	-9.0	-8.5	V	1

Notes:
1. FDL can use the same supply as Vertical CCD Clocks Low if desired.

Clock Line Capacitances

Clocks	Capacitance	Units	Notes
V1 to GND	108	nF	1
V2 to GND	118	nF	1
V1 to V2	56	nF	
H1S to GND	27	pF	2
H2S to GND	27	pF	2
H1B to GND	13	pF	2
H2B to GND	4	pF	2
H1S to H2B and H2S	13	pF	2
H1B to H2B and H2S	13	pF	2
H2S to H1B and H1S	13	pF	2
H2B to H1B and H1S	13	pF	2
H1BIN to GND	20	pF	2
R to GND	10	pF	
FD to GND	20	pF	

Notes:
1. Gate capacitance to GND is voltage dependent. Value is for nominal VCCD clock voltages.
2. For nominal HCCD clock voltages, these values are for half of the imager (H1SL, H1BL, H2SL, H2BL and H1BINL or H1SR, H1BR, H2SR, H2BR and H1BINR).

Timing Requirements

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
HCCD Delay	T_{HD}	3.0	3.5	10.0	µs	
VCCD Transfer time	T_{VCCD}	3.0	3.5	20.0	µs	
Photodiode Transfer time	T_{V3rd}	8.0	10.0	15.0	µs	
VCCD Pedestal time	T_{3P}	100.0	120.0	200.0	µs	
VCCD Delay	T_{3D}	15.0	20.0	80.0	µs	
Reset Pulse time	T_R	2.5	5.0		ns	
Shutter Pulse time	T_S	3.0	4.0	10.0	µs	
Shutter Pulse delay	T_{SD}	1.0	1.5	10.0	µs	
HCCD Clock Period	T_H	33		200	ns	
VCCD rise/fall time	T_{VR}	0.0	0.1	1.0	µs	
Fast Dump Gate delay	T_{FD}	0.5			µs	
Vertical Clock Edge Alignment	T_{VE}	0.0		100	ns	

Notes:

Main Timing – Continuous Mode

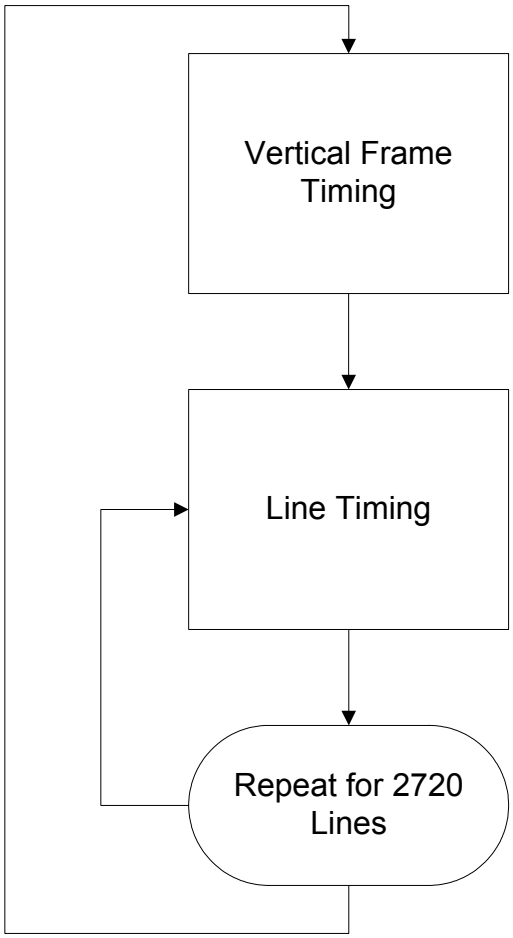


Figure 13 - Main Timing - Continuous Mode

Frame Timing – Continuous Mode

Frame Timing without Binning

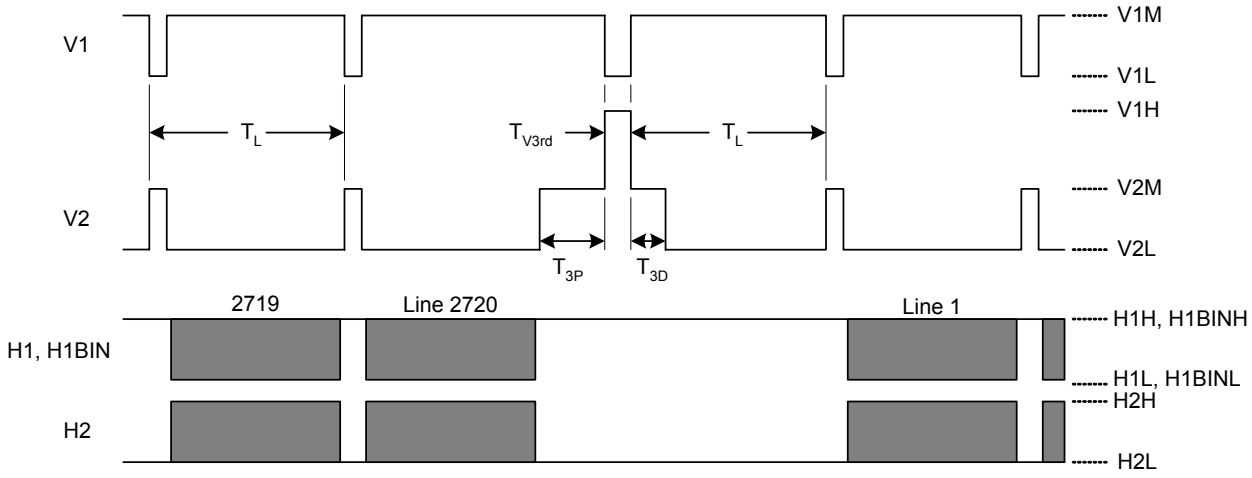


Figure 14 - Framing Timing without Binning

Frame Timing for Vertical Binning by 2

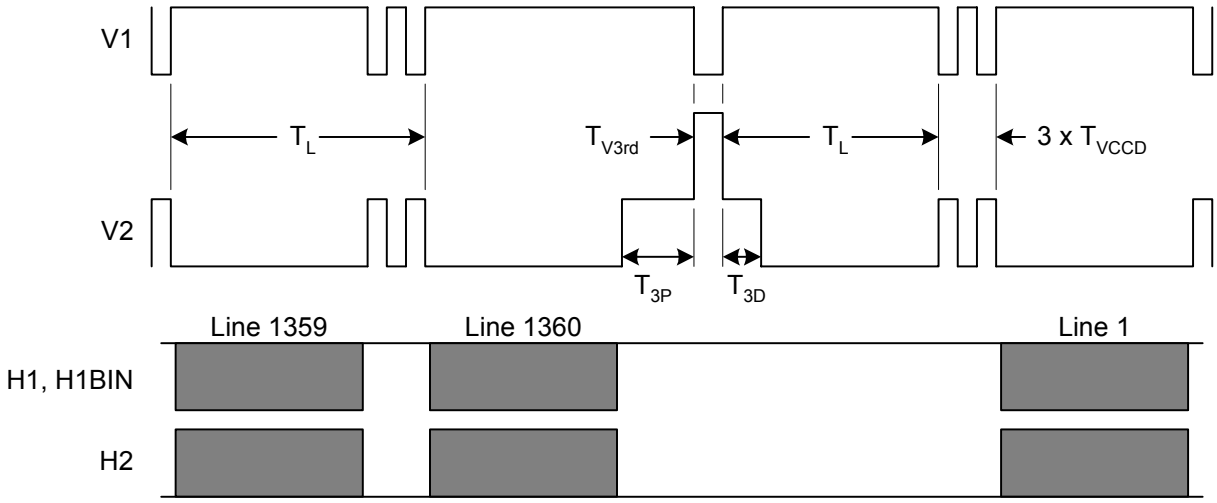


Figure 15 - Frame Timing for Vertical Binning by 2

Frame Timing Edge Alignment

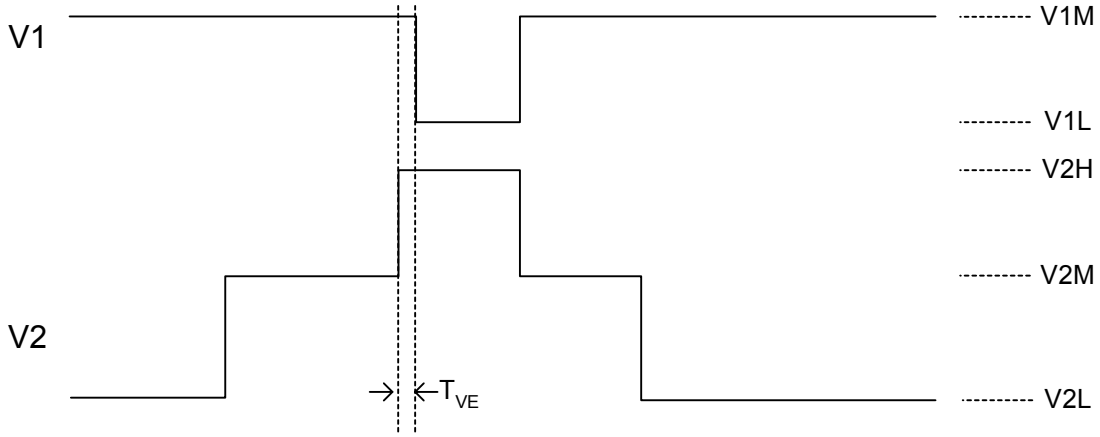


Figure 16 - Frame Timing Edge Alignment

Line Timing – Continuous Mode

Line Timing Single Output

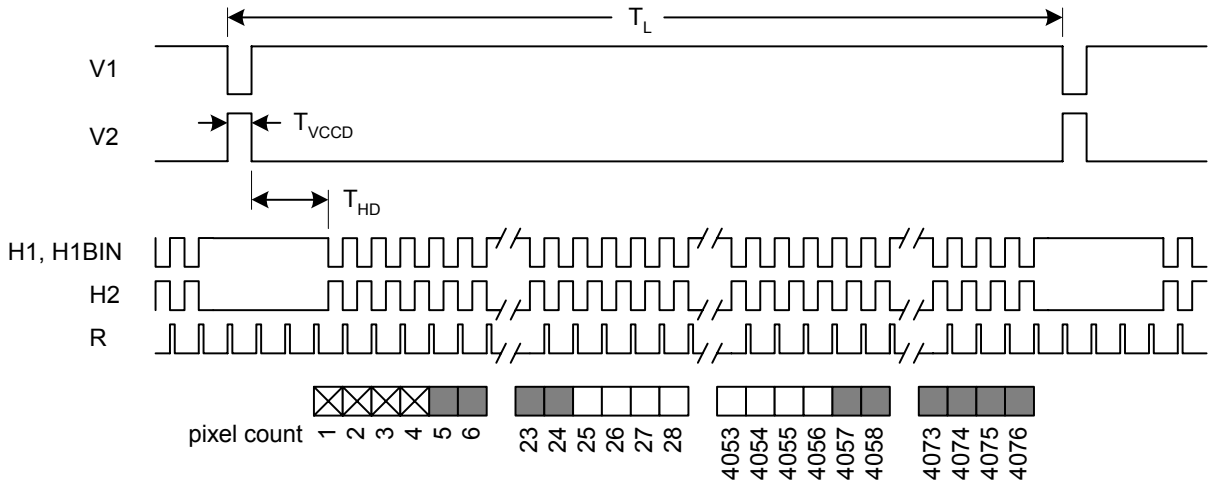


Figure 17 - Line Timing Single Output

Line Timing Dual Output

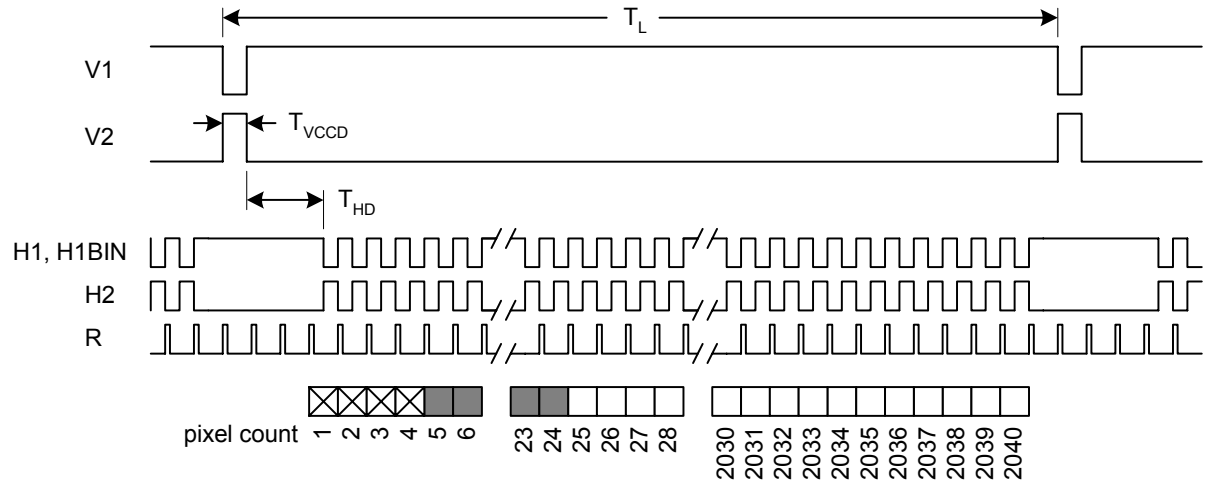


Figure 18 - Line Timing Dual Output

Line Timing Vertical Binning by 2

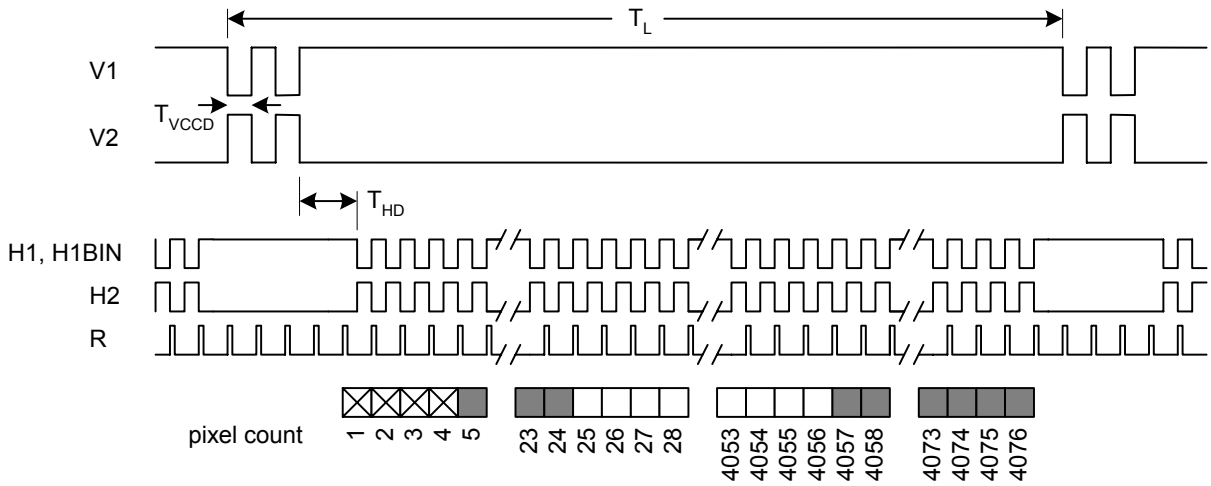


Figure 19 - Line Timing Vertical Binning by 2

Line Timing Detail

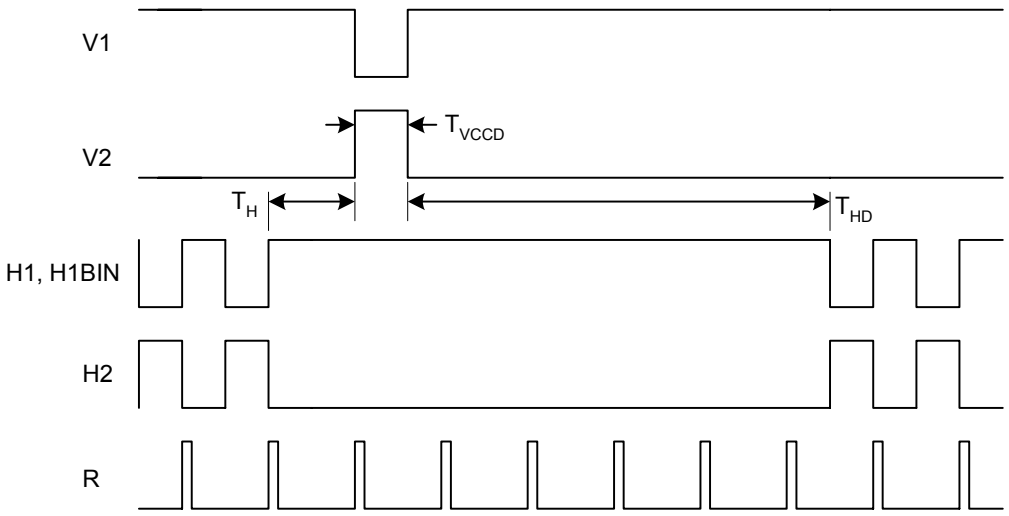


Figure 20 - Line Timing Detail

Line Timing Binning by 2 Detail

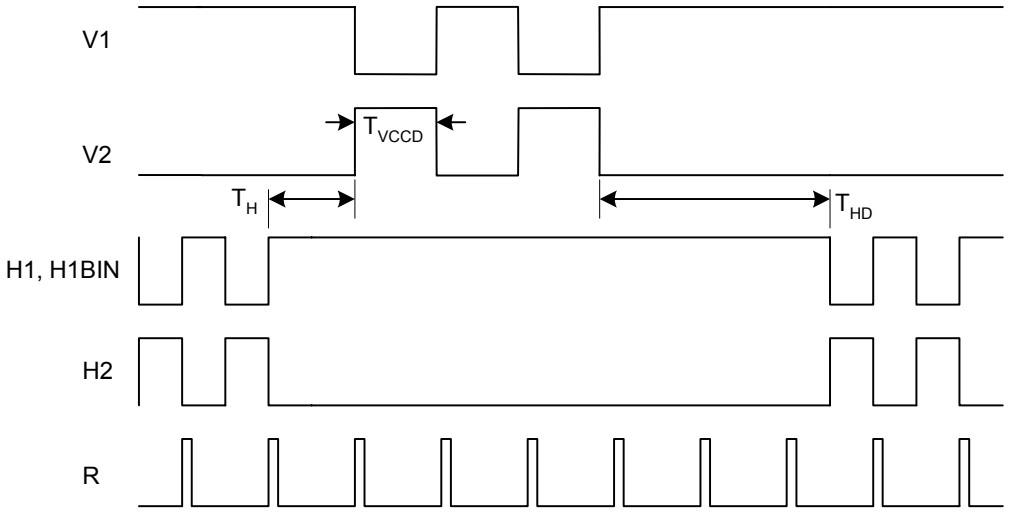


Figure 21 - Line Timing by 2 Detail

Line Timing Edge Alignment

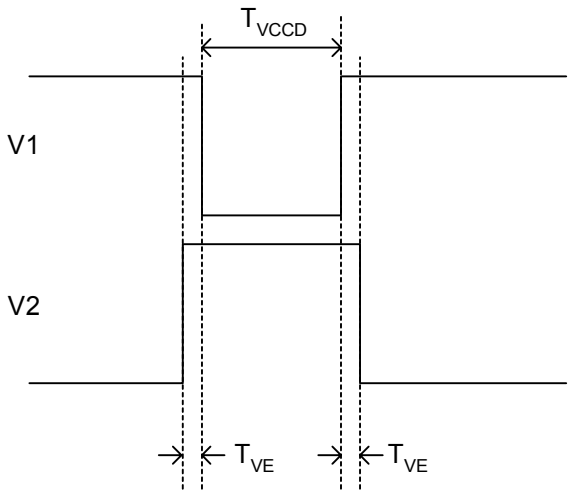


Figure 22 - Line Timing Edge Alignment

Pixel Timing – Continuous Mode

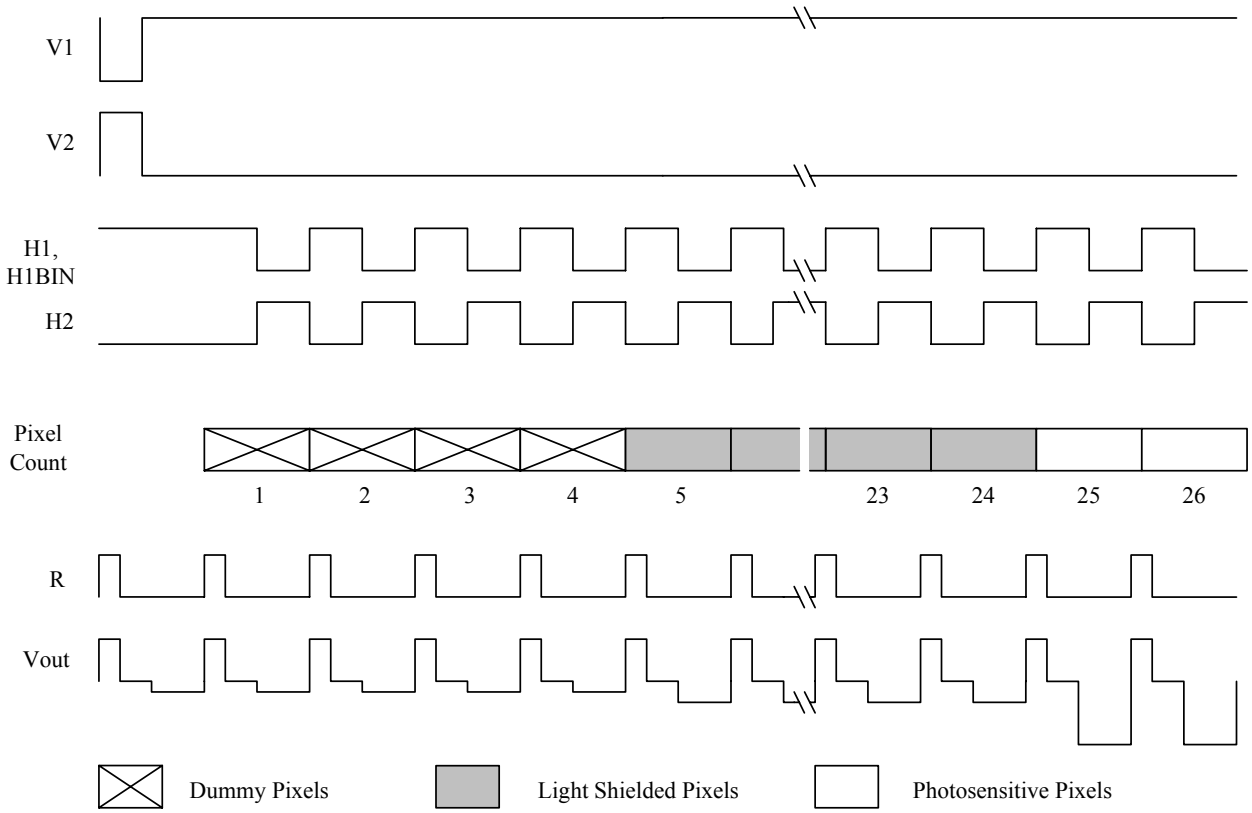


Figure 23 - Pixel Timing

Pixel Timing Detail

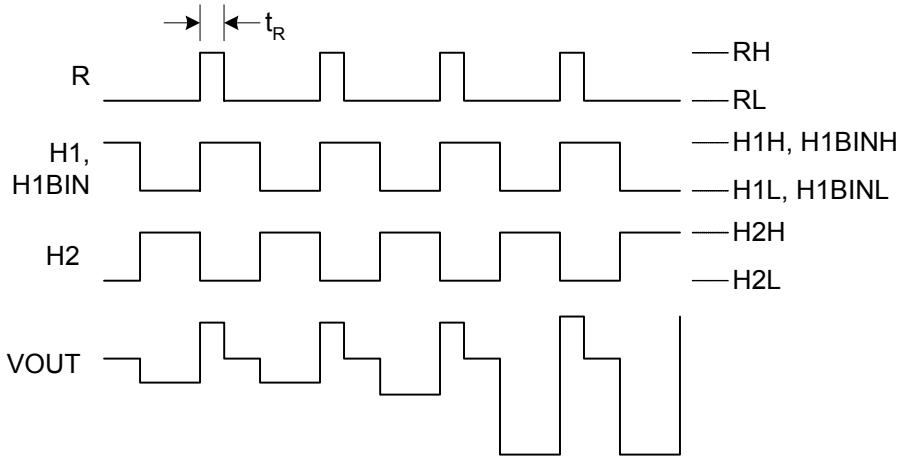


Figure 24 - Pixel Timing Detail

Fast Line Dump Timing

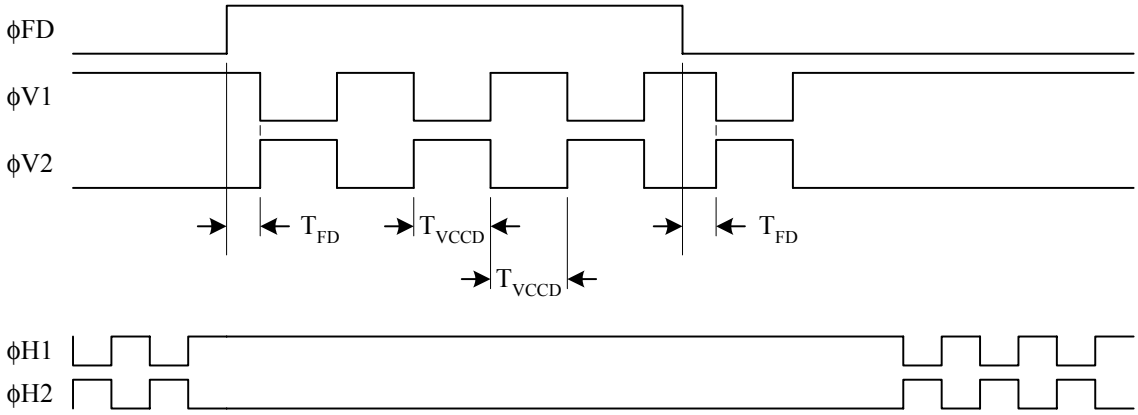


Figure 25 - Fast Line Dump Timing

Electronic Shutter

Electronic Shutter Line Timing

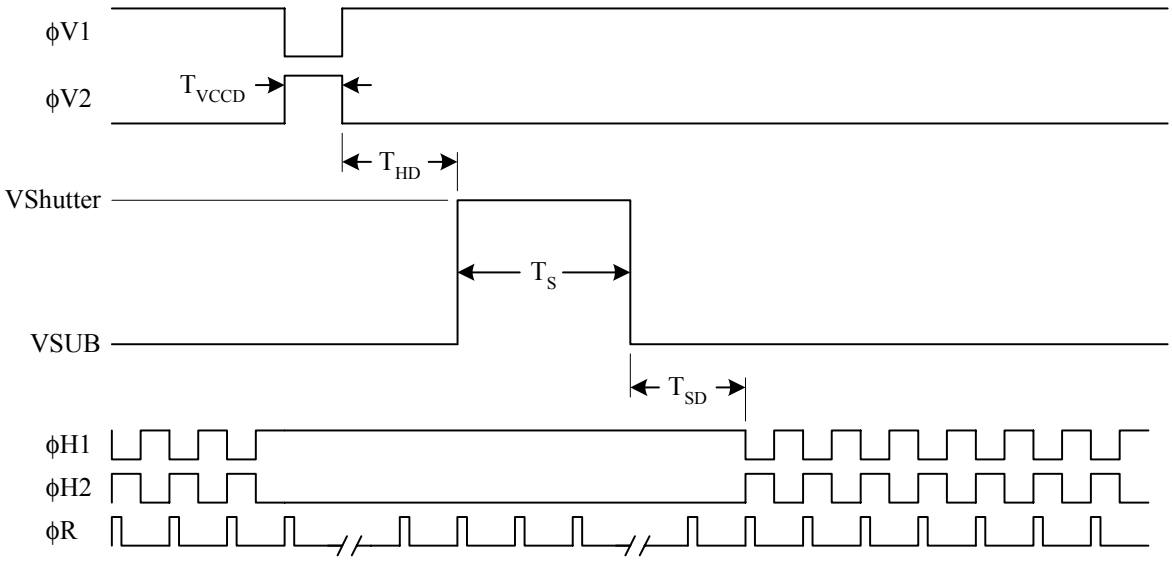


Figure 26 - Electronic Shutter Line Timing

Electronic Shutter – Integration Time Definition

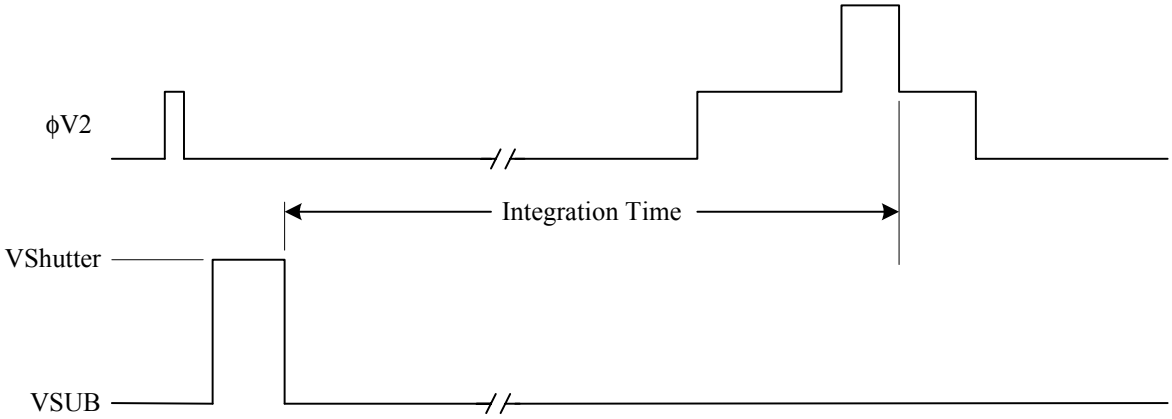


Figure 27 - Integration Time Definition

Electronic Shutter Description

The voltage on the substrate (SUB) determines the charge capacity of the photodiodes. When SUB is 8 volts the photodiodes will be at their maximum charge capacity. Increasing VSUB above 8 volts decreases the charge capacity of the photodiodes until 40 volts when the photodiodes have a charge capacity of zero electrons. Therefore, a short pulse on SUB, with a peak amplitude greater than 40 volts, empties all photodiodes and provides the electronic shuttering action.

It may appear the optimal substrate voltage setting is 8 volts to obtain the maximum charge capacity and dynamic range. While setting VSUB to 8 volts will provide the maximum dynamic range, it will also provide the minimum antiblooming protection.

The KAI-11000 VCCD has a charge capacity of 90,000 electrons (90 ke^-). If the SUB voltage is set such that the photodiode holds more than 90 ke^-, then when the charge is transferred from a full photodiode to VCCD, the VCCD will overflow. This overflow condition manifests itself in the image by making bright spots appear elongated in the vertical direction. The size increase of a bright spot is called blooming when the spot doubles in size.

The blooming can be eliminated by increasing the voltage on SUB to lower the charge capacity of the photodiode. This ensures the VCCD charge capacity is greater than the photodiode capacity. There are cases where an extremely bright spot will still cause blooming in the VCCD. Normally, when the photodiode is full, any additional electrons generated by photons will spill out of the photodiode. The excess electrons are drained harmlessly out to the substrate. There is a maximum rate at which the electrons can be drained to the substrate. If that maximum rate is exceeded, (for example, by a very bright light source) then it is possible for the total amount of charge in the photodiode to exceed the VCCD capacity. This results in blooming.

The amount of antiblooming protection also decreases when the integration time is decreased. There is a compromise between photodiode dynamic range (controlled by VSUB) and the amount of antiblooming protection. A low VSUB voltage provides the maximum dynamic range and minimum (or no) antiblooming protection. A high VSUB voltage provides lower dynamic range and maximum antiblooming protection. The optimal setting of VSUB is written on the container in which each KAI-11000 is shipped. The given VSUB voltage for each sensor is selected to provide antiblooming protection for bright spots at least 100 times saturation, while maintaining at least 70 ke^- of dynamic range.

The electronic shutter provides a method of precisely controlling the image exposure time without any mechanical components. If an integration time of T_{INT} is desired, then the substrate voltage of the sensor is pulsed to at least 40 volts T_{INT} seconds before the photodiode to VCCD transfer pulse on V2. Use of the electronic shutter does not have to wait until the previously acquired image has been completely read out of the VCCD.

STORAGE AND HANDLING

Storage Conditions

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-20	80	°C	1
Humidity	RH	5	90	%	2

Notes:
1. Long-term exposure toward the maximum temperature will accelerate color filter degradation.
2. T=25ºC. Excessive humidity will degrade MTTF.

Soldering Recommendations

1. The soldering iron tip temperature is not to exceed 370ºC. Failure to do so may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating. Kodak recommends the use of a grounded 30W soldering iron. Heat each pin for less than 2 seconds duration.

MECHANICAL DRAWINGS

Package

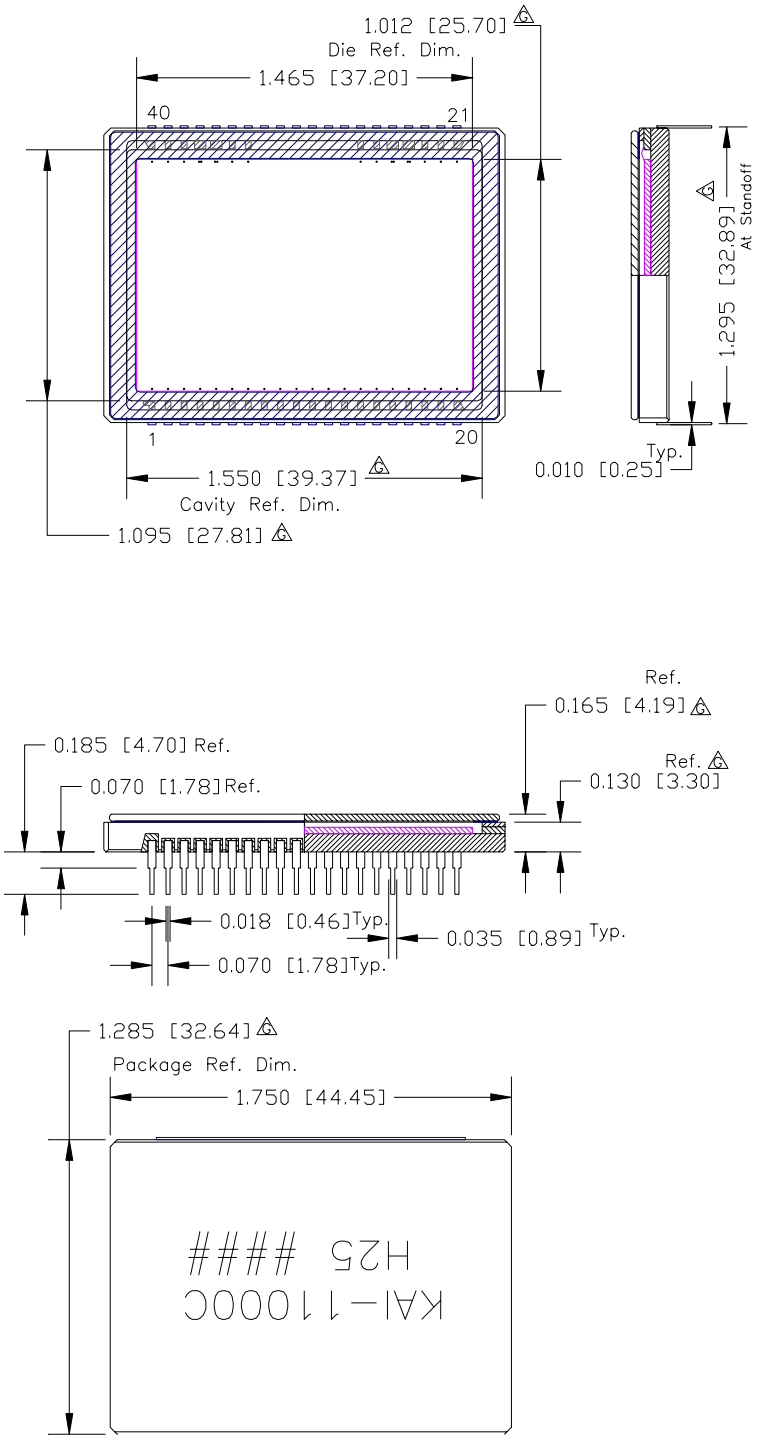
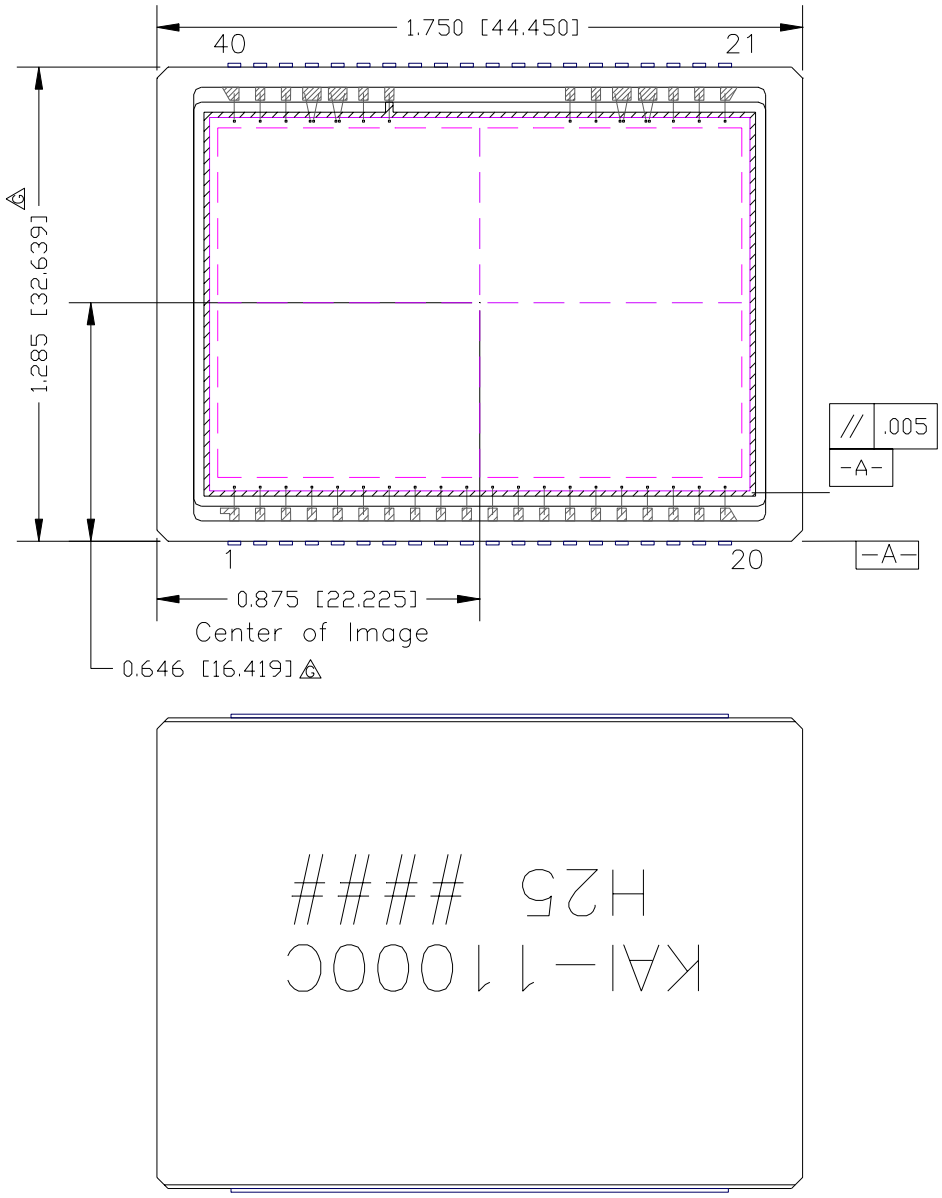


Figure 28 - Package Drawing

Die to Package Alignment

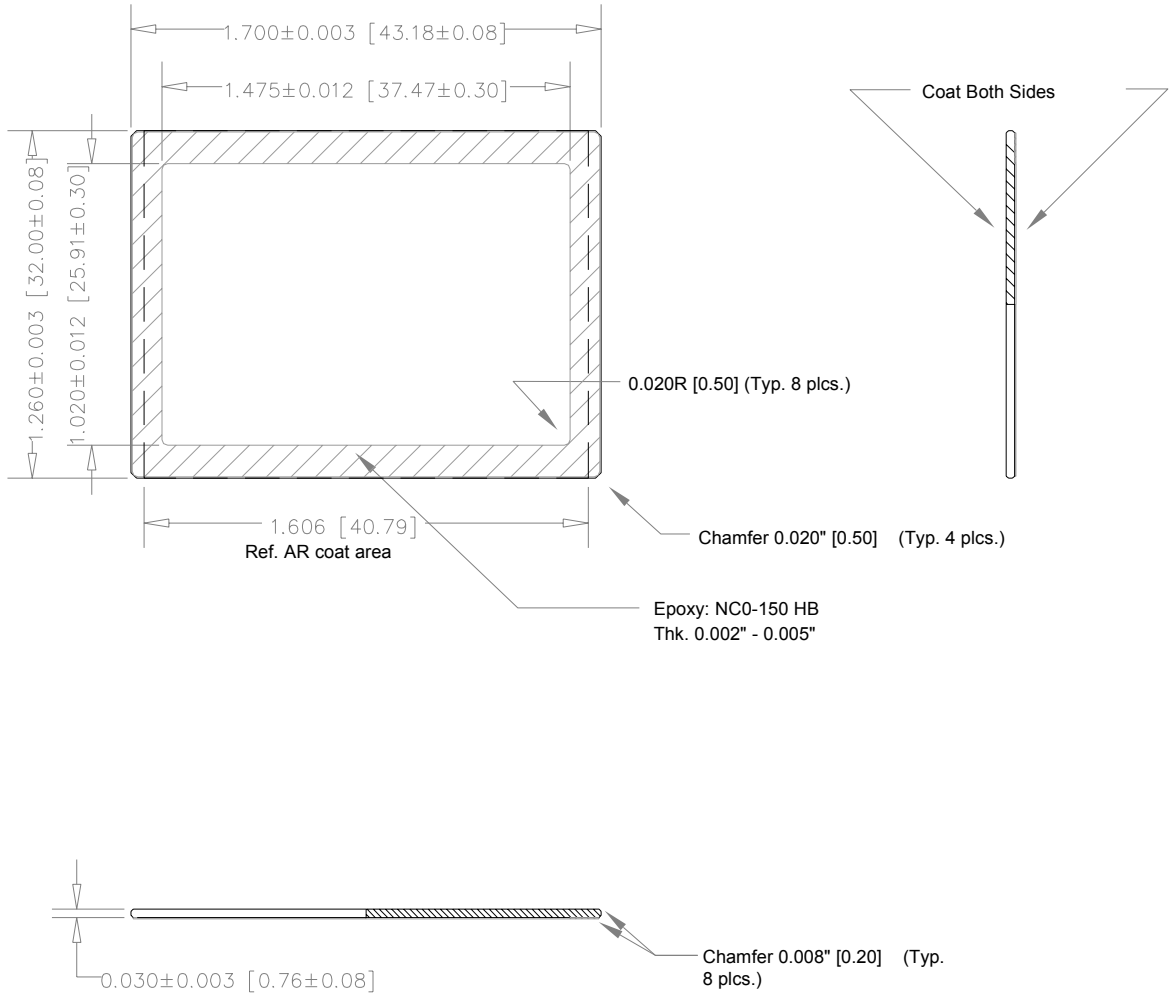


Notes:

1. Center of image is offset from center of package by (0.00,0.01)cm

Figure 29 - Die to Package Alignment

Glass



NOTES:

1. Multi-Layer Anti-Reflective Coating on 2 sides:
   Double Sided Reflectance:
   Range (nm)
   420 - 450 nm < 2%
   450 - 630 nm < 1%
   630 - 680 nm < 2%
2. Dust, Scratch specification - 20 microns max.
3. Substrate - Schott D-263 or Equivalent
4. Epoxy: NCO-150HB
   Thickness: 0.002" - 0.005"

Figure 30 - Glass Drawing

Glass Transmission

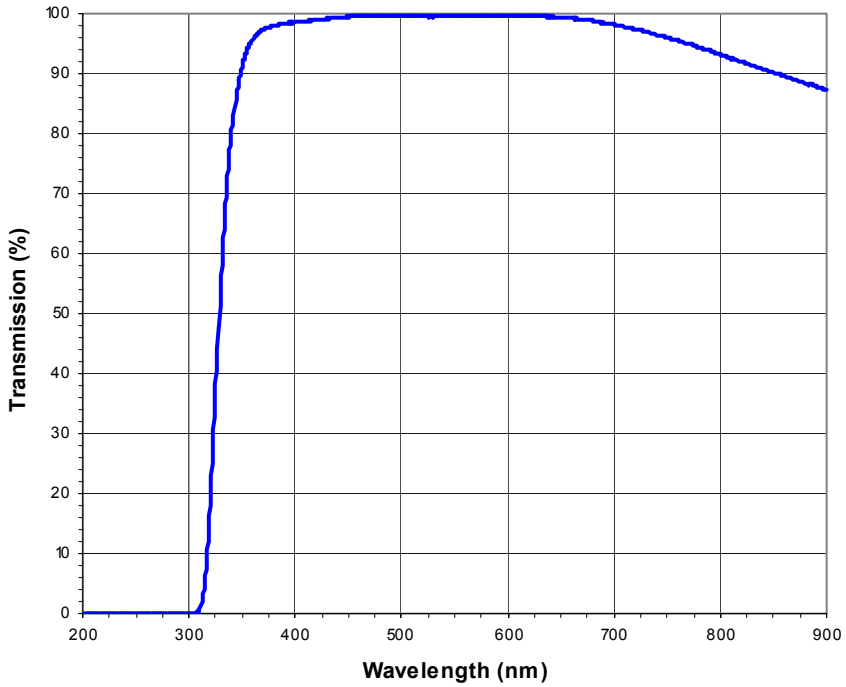


Figure 31 – AR Glass Transmission

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD) damage, or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note MTD/PS-0237, Cover Glass Cleaning for Image Sensors, for further information.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224, Electrostatic Discharge Control, for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

Available Part Configurations

Type	Description	Glass Configuration
KAI-11000M	Monochrome with microlens	Sealed AR Coated Both Sides
KAI-11000CM	Color with microlens	Sealed AR Coated Both Sides

Please contact Image Sensor Solutions for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

REVISION CHANGES

Revision Number	Description of Changes
1	Initial formal release
2	Page 16 - Addition of class 1 defect description.
3	Removed Low Dark Current Mode Removed IR Glass option Page 16: Defect class definitions changed Class 1: Monochrome or Color Class 2: Color only Page 23: Changed VCCD Pedestal time, T3p values was (50,60,80), now (100,120,200) for min, nom, max Page 21: A caution was added for cover glass protective tape that is used on each sensor. Page 38: Changed glass drawing from IR to MAR.